MIXTILE

Core 3588E | System on Module

Data Sheet V2.1.0

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Change history

Version	Date	Changes
1.0	2023-08-24	First version
1.1	2023-11-02	Added description about the heatsink fan as an optional accessory.
2.0.0	2025-12-19	Updated the product image of Core 3588E and modified the interface.
2.1.0	2026-06-10	Changed the pin connection of CSI 0 and CSI 1, reversed the positions of the D0 signal and the D2 signal in Display Port 1. Purpose: To be compatible with Jeston Orin Nano carrier board.

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1. Overview

Mixtile Core 3588E is a compact SoM powered by Rockchip RK3588, a high-performance low-power AIoT processor that integrates quad-core Cortex-A76 and quad-core Cortex-A55. Capable of delivering up to 6 TOPS AI performance, Core 3588E targets a wide range of applications, including ARM-based PCs, Edge Computing devices, personal mobile internet devices, and other digital multimedia applications.

2. Main features

- Excellent video processing capabilities
  - 8Kp60 video decoding (H.264/H.265/VP9)
  - 8Kp30 video encoding (H.264/H.265)
  - JPEG encoding and decoding
- Robust image processing capabilities
  - High Dynamic Range (HDR)
  - 3A
  - LSC
  - 3DNR, 2DNR
  - Sharpening
  - Dehaze
  - Fisheye correction
  - Gamma correction
  - Image preprocessor and postprocessor
- Strong AI performance
  - 6 TOPS
  - INT4/INT8/INT16/FP16
  - TensorFlow/MXNet/PyTorch/Caffe
- High-speed interfaces: PCIe 3.0 x4 lanes + PCIe 2.1 x1 lane

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3. Technical specifications

Technical items		Specifications
General	CPU	Quad-core Cortex-A76 (2.4 GHz) + Quad-core Cortex-A55, Neon and FPU
	GPU	Arm Mali-G610 MP4 with support for OpenGL ES3.2, OpenCL 2.2, Vulkan1.2
	NPU	RK NN, 6 TOPS NPU with support for TensorFlow, Caffe, TFLite, PyTorch, ONNX NN, Android NN
	Memory	4 GB, 8 GB, 16 GB, or 32 GB 64-bit LPDDR5X
	Storage	32 GB, 64 GB, or 128 GB eMMC 5.1 flash storage
	Supported OS	Debian 11, Android 11, Ubuntu 22.04, and Armbian 23.07
	Supply power	5 V DC
	Video codec	8Kp60 video decoding (H.264/H.265/VP9) 8Kp30 video encoding (H.264/H.265)
	ISP	48M ISP, HDR
	OTP	Size: 8K
Interfaces	Display	1x DP/eDP/HDMI interface + 1x DP/eDP/USB3.0 combo interface, up to 7680 x 4320@60 Hz for HDMI and DP, and 3840 x 2160@60 Hz for eDP
	Camera	2x 4-lane or 5x 2-lane MIPI CSI interfaces @ 2.5 Gbps/lane
	Network	2.5G BASE-T
	USB	2x USB 3.0 (Gen1), 3x USB 2.0
	PCIe	PCIe 3.0 x4 + 2x PCIe 2.1 x1
	Others	• UART DEBUG x1, UART+flow control x2 • SPI x2 • I^2C x4 • CAN x1 • I^2S x4 • PWM x3, GPIO x9
Mechanical	Connector	260-pin SO-DIMM edge connector, compatible with Jetson TX2 NX
	Optional accessory	Heatsink fan
	Dimensions	69.6 mm x 45 mm
Environment	Temperature	• Operating: 0°C to 80°C • Storage: -20°C to 85°C
	Relative humidity	• Operating: 10% to 90% • Storage: 5% to 95%

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4. Functional description

4.1 Microprocessor

- Quad-core ARM Cortex-A76 MPCore processor and quad-core ARM Cortex-A55 MPCore processor, both are high-performance, low-power and cached application processors
- DSU (DynamIQ Shared Unit) comprises the L3 memory system, control logic, and external interfaces to support a DynamIQ cluster
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- TrustZone technology support
- Integrated 64KB L1 instruction cache, 64KB L1 data cache and 512KB L2 cache for each Cortex-A76
- Integrated 32KB L1 instruction cache, 32KB L1 data cache and 128KB L2 cache for each Cortex-A55
- Quad-core Cortex-A76 and Quad-core Cortex-A55 share 3MB L3 cache
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenarios:
  - PD_CPU_0: 1st Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_1: 2nd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_2: 3rd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_3: 4th Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_4: 1st Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_5: 2nd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_6: 3rd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_7: 4th Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
- Three isolated voltage domains to support DVFS, one for A76_0 and A76_1, one for A76_2 and A76_3, the other for DSU and Cortex-A55

4.2 Memory organization

- Internal on-chip memory
  - BootRom
    - Support system boot from the following interfaces:
      - SPI interface
      - eMMC interface
      - SD/MMC interface
    - Support system code download by the following interface:
      - USB OTG interface
  - Share Memory in the voltage domain of VD_LOGIC
  - PMU SRAM in VD_PMU for low power application
- External off-chip memory

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- Dynamic Memory Interface
  - Compatible with JEDEC standards LPDDR4/LPDDR4X/LPDDR5/LPDDR5X
  - Support four channels, 16 bits data widths for each channel
  - Support up to 2 ranks (chip selects) for each channel
  - Totally up to 32 GB address space
  - Low power modes, such as power-down and self-refresh for SDRAM
- eMMC Interface
  - Fully compliant with JEDEC eMMC 5.1 and eMMC 5.0 specification
  - Backward compliant with eMMC 4.51 and earlier versions specification
  - Support HS400, HS200, DDR50 and legacy operating modes
  - Support three data bus widths: 1 bit, 4 bits, and 8 bits
- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Data bus width is 4 bits
- Flexible Serial Flash Interface
  - Support transferring data from/to serial flash device
  - Support 1 bit, 2 bits or 4 bits data bus width
  - Support 2 chips select

4.3 System components

- MCU (microcontroller unit)
  - Three Cortex-M0 MCUs inside RK3588:
    - MCU in VD_PMU integrate 16KB Cache and 16KB TCM
    - MCU in VD_NPU integrate 16KB Cache and 64KB TCM
    - MCU in PD_CENTER integrate 32KB TCM
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU in VD_PMU(PMU_M0) and PD_CENTER(DDR_M0)
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support total 18 PLLs to generate all clocks
  - One oscillator with 24 MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different modes
  - Support 10 separate voltage domains
  - Support 45 separate power domains, which can be powered up/down by software based on different application scenes
- Timer
  - Support 12 secure timers with 64 bits counter and interrupt-based operation

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- Support 18 non-secure timers with 64 bits counter and interrupt-based operation
- Support two operation modes: free-running and user-defined count for each timer
- Support timer work state checkable

- PWM
  - Support 16 on-chip PWMs (PWM0~PWM15) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provide reference mode and output various duty-cycle waveforms
  - Optimized for IR application for PWM3, PWM7, PWM11, PWM15
- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - Watchdog timer (WDT) can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt. If this is not cleared by the service routine by the time a second timeout occurs, then generate a system reset
  - Totally five watchdogs for CPU and MCU
- Interrupt controller
  - Support 12 PPI interrupt sources and 480 SPI interrupt sources input from different components inside RK3588
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support different interrupt priorities for each interrupt source, and they are always software-programmable
- DMAC
  - Micro-code programming based DMA
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
  - Totally three embedded DMA controllers for peripheral system
  - Features of each DMAC:
    - Support 8 channels
    - 32 hardware request from peripherals
    - 2 interrupt output
    - Support TrustZone technology and programmable secure state for each DMA channel
- Secure system
  - Embedded two cipher engines
    - Support Link List Item (LLI) DMA transfer
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5, SM3 with hardware padding
    - Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode

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- Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES & TDES cipher, with ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
- Support generating random numbers

- Support keyladder to guarantee key secure
- Support data scrambling for all DDR types
- Support secure OTP
- Support secure debug
- Support secure DFT test
- Support secure OS
- Except CPU, the other masters in the SoC can also support security and non- security mode by software-programmable
- Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
- System SRAM (share memory), part of space is addressed only in security mode
- External DDR space can be divided into 16 parts, each part can be software-programmable to be enabled by each master

- Mailbox
  - Three mailboxes in SoC to service CPU and MCU communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- Decompression
  - Support decompressing GZIP files
  - Support decompressing LZ4 files, including the General Structure of LZ4 Frame format and the Legacy Frame format
  - Support decompressing data in DEFLATE format
  - Support decompressing data in ZLIB format
  - Support Hash32 check in LZ4 decompression process
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

4.4 Video codec

- Video decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC, AV1
  - MMU Embedded
  - Multi-channel decoder in parallel for less resolution
  - H.264 AVC/MVC Main10 L6.0 : 8K@30fps (7680 x 4320)[2]
  - VP9 Profile0/2 L6.1 : 8K@60fps (7680 x 4320)
  - H.265 HEVC/MVC Main10 L6.1 : 8K@60fps (7680 x 4320)
  - AVS2 Profile0/2 L10.2.6 : 8K@60fps (7680 x 4320)

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- AV1 Main Profile 8/10bit L5.3. : 4K@60fps (3840 x 2160)
- MPEG-2 up to MP : 1080p@60fps (1920 x 1088)
- MPEG-1 up to MP : 1080p@60fps (1920 x 1088)
- VC-1 up to AP level 3 : 1080p@60fps (1920 x 1088)
- VP8 version2 : 1080p@60fps (1920 x 1088)

- Video encoder
  - Real-time H.265/H.264 video encoding
  - Support up to 8K@30fps
  - Multi-channel encoder in parallel for less resolution

4.5 JPEG codec

- JPEG encoder
  - Baseline (DCT sequential)
  - Encoder size is from 96 x 96 to 8192 x 8192 (67 Mpixels)
  - Up to 90 million pixels per second
  - Embedded four encoder units
- JPEG decoder
  - Decoder size is from 48 x 48 to 65536 x 65536
  - Support YUV400/YUV411/YUV420/YUV422/YUV440/YUV444
  - Support up to 1080P@280fps, and 560 million pixels per second
  - Support MJPEG
  - Embedded four encoder units

4.6 Neural process unit

- Neural network acceleration engine with processing performance up to 6 TOPS
- Include triple NPU core, and support triple core co-work, dual core co-work, and work independently
- Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation
- Embedded 384KBx3 internal buffer
- Multi-task, multi-scenario in parallel
- Support deep learning frameworks: TensorFlow, Caffe, TFlite, PyTorch, ONNX NN, Android NN, etc.
- One isolated voltage domain to support DVFS

4.7 Graphics engine

- 3D graphics engine
  - ARM Mali-G610 MP4
  - High performance OpenGLES 1.1, 2.0 and 3.2, OpenCL 2.2, Vulkan1.2 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 4x 256 KB size
  - The latest Valhall architecture

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- ARM Frame Buffer Compression (AFBC) 1.3
- Support Serial Wire debug for embedded MCU
- One isolated voltage domain to support DVFS

- 2D graphics engine
  - Source format: ARGB/RGB888/RGB565/YUV420/YUV422/BPP
  - Destination formats: ARGB/RGB888/RGB565/YUV420/YUV422
  - Max resolution: 8192 x 8192 source, 4096 x 4096 destination
  - Block transfer and transparency mode
  - Color fill with gradient fill, and pattern fill
  - Alpha blending modes including global alpha, per pixel alpha (color/alpha channel separately) and fading
  - Arbitrary non-integer scaling ratio, from 1/8 to 8
  - 0, 90, 180, 270 degree rotation, x-mirror, y-mirror & rotation operation
  - ROP2, ROP3, ROP4
  - Support 4k/64k page size MMU
- Image enhancement processor
  - Image format
    - Input data: YUV420/YUV422, semi-planar/planar, UV swap
    - Output data: YUV420/YUV422, semi-planar, UV swap, Tile mode
    - YUV down sampling conversion from 422 to 420
    - Max resolution for dynamic image up to 1920 x 1080
  - De-interlace

4.8 Video input interface

- MIPI interface
  - Two MIPI DC (DPHY/CPHY) combo PHY
    - Support to use DPHY or CPHY
    - Each MIPI DPHY V2.0, 4 lanes, 4.5 Gbps per lane
    - Each MIPI CPHY V1.1, 3 lanes, 2.5 Gbps per lane
  - Four MIPI CSI DPHY
    - Each MIPI DPHY V1.2, 2 lanes, 2.5 Gbps per lane
    - Support to combine 2 DPHY together to one 4-lane
  - Support camera input combination
    - 2 MIPI DCPHY + 4 MIPI CSI DPHY (2 lanes), totally support 6 cameras input
    - 2 MIPI DCPHY + 1 MIPI CSI DPHY (4 lanes) + 2 MIPI CSI DPHY (2 lanes), totally support 5 cameras input
    - 2 MIPI DCPHY + 2 MIPI CSI DPHY (4 lanes), totally support 4 cameras input
  - Notice
    - In version 2.1.0, the PCB design connects the CSI0 signal to the CSI1 interface definition, and then the CSI1 signal is connected to the CSI0 interface definition.
    - When performing the 4Line operation using CSI0 and CSI1, the clock must use CSI0_CLK.
    - When performing the 4Line operation using CSI2 and CSI3, the clock must use

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CSI2_CLK.

Pin #	Pin name	Signal description	Direction	Pin type
3	CSI1_D0_N	Camera, CSI 0 Data 0–	Input	MIPI D-PHY
5	CSI1_D0_P	Camera, CSI 0 Data 0+	Input	MIPI D-PHY
9	CSI1_CLK_N	Camera, CSI 0 Clock–	Input	MIPI D-PHY
11	CSI1_CLK_P	Camera, CSI 0 Clock+	Input	MIPI D-PHY
15	CSI1_D1_N	Camera, CSI 0 Data 1–	Input	MIPI D-PHY
17	CSI1_D1_P	Camera, CSI 0 Data 1+	Input	MIPI D-PHY
4	CSI0_D0_N	Camera, CSI 1 Data 0–	Input	MIPI D-PHY
6	CSI0_D0_P	Camera, CSI 1 Data 0+	Input	MIPI D-PHY
10	CSI0_CLK_N	Camera, CSI 1 Clock–	Input	MIPI D-PHY
12	CSI0_CLK_P	Camera, CSI 1 Clock+	Input	MIPI D-PHY
16	CSI0_D1_N	Camera, CSI 1 Data 1–	Input	MIPI D-PHY
18	CSI0_D1_P	Camera, CSI 1 Data 1+	Input	MIPI D-PHY
22	CSI2_D0_N	Camera, CSI 2 Data 0–	Input	MIPI D-PHY
24	CSI2_D0_P	Camera, CSI 2 Data 0+	Input	MIPI D-PHY
28	CSI2_CLK_N	Camera, CSI 2 Clock–	Input	MIPI D-PHY
30	CSI2_CLK_P	Camera, CSI 2 Clock+	Input	MIPI D-PHY
34	CSI2_D1_N	Camera, CSI 2 Data 1–	Input	MIPI D-PHY
36	CSI2_D1_P	Camera, CSI 2 Data 1+	Input	MIPI D-PHY
21	CSI3_D0_N	Camera, CSI 3 Data 0–	Input	MIPI D-PHY
23	CSI3_D0_P	Camera, CSI 3 Data 0+	Input	MIPI D-PHY
27	CSI3_CLK_N	Camera, CSI 3 Clock–	Input	MIPI D-PHY
29	CSI3_CLK_P	Camera, CSI 3 Clock+	Input	MIPI D-PHY
33	CSI3_D1_N	Camera, CSI 3 Data 1–	Input	MIPI D-PHY
35	CSI3_D1_P	Camera, CSI 3 Data 1+	Input	MIPI D-PHY
58	CSI4_D0_N	Camera, CSI 4 Data 0–	Input	MIPI D-PHY
60	CSI4_D0_P	Camera, CSI 4 Data 0+	Input	MIPI D-PHY
64	CSI4_D1_N	Camera, CSI 4 Data 1–	Input	MIPI D-PHY
66	CSI4_D1_P	Camera, CSI 4 Data 1+	Input	MIPI D-PHY
70	CSI4_CLK_N	Camera, CSI 4 Clock–	Input	MIPI D-PHY
72	CSI4_CLK_P	Camera, CSI 4 Clock+	Input	MIPI D-PHY
76	CSI5_D0_N	Camera, CSI 5 Data 0–	Input	MIPI D-PHY
78	CSI5_D0_P	Camera, CSI 5 Data 0+	Input	MIPI D-PHY
82	CSI5_D1_N	Camera, CSI 5 Data 1–	Input	MIPI D-PHY
84	CSI5_D1_P	Camera, CSI 5 Data 1+	Input	MIPI D-PHY
88	CSI5_CLK_N	Camera, CSI 5 Clock–	Input	MIPI D-PHY

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Pin #	Pin name	Signal description	Direction	Pin type
90	CSI5_CLK_P	Camera, CSI 5 Clock+	Input	MIPI D-PHY

Table 1. CSI pin descriptions

Pin #	Signal description	Pin Delay	
		Pin 1	Pin 2
3	Camera, CSI 0 Data 0–		0.0637508 ns
5	Camera, CSI 0 Data 0+		0.0655029 ns
9	Camera, CSI 0 Clock–		0.0802524 ns
11	Camera, CSI 0 Clock+		0.0795411 ns
15	Camera, CSI 0 Data 1–	0.066243 ns	
17	Camera, CSI 0 Data 1+	0.0673719 ns	
4	Camera, CSI 1 Data 0–		0.07644 ns
6	Camera, CSI 1 Data 0+		0.075635 ns
10	Camera, CSI 1 Clock–		0.0730463 ns
12	Camera, CSI 1 Clock+		0.0724097 ns
16	Camera, CSI 1 Data 1–		0.071983 ns
18	Camera, CSI 1 Data 1+		0.0715445 ns
22	Camera, CSI 2 Data 0–	0.0584158 ns	
24	Camera, CSI 2 Data 0+	0.0582208 ns	
28	Camera, CSI 2 Clock–	0.0630604 ns	
30	Camera, CSI 2 Clock+	0.0623516 ns	
34	Camera, CSI 2 Data 1–	0.0691472 ns	
36	Camera, CSI 2 Data 1+	0.0724909 ns	
21	Camera, CSI 3 Data 0–		0.0634245 ns
23	Camera, CSI 3 Data 0+		0.0631321 ns
27	Camera, CSI 3 Clock–	0.0703476 ns	
29	Camera, CSI 3 Clock+	0.0704478 ns	
33	Camera, CSI 3 Data 1–	0.0613721 ns	
35	Camera, CSI 3 Data 1+	0.0611174 ns	
58	Camera, CSI 4 Data 0–	0.0559165 ns	
60	Camera, CSI 4 Data 0+	0.0546732 ns	
64	Camera, CSI 4 Data 1–	0.0629527 ns	
66	Camera, CSI 4 Data 1+	0.0573681 ns	
70	Camera, CSI 4 Clock–	0.0618566 ns	
72	Camera, CSI 4 Clock+	0.0642331 ns	
76	Camera, CSI 5 Data 0–	0.0296462 ns	
78	Camera, CSI 5 Data 0+	0.0258709 ns	
82	Camera, CSI 5 Data 1–	0.030861 ns	

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Pin #	Signal description	Pin Delay	
		Pin 1	Pin 2
84	Camera, CSI 5 Data 1+	0.0239932 ns	
88	Camera, CSI 5 Clock–	0.0291243 ns	
90	Camera, CSI 5 Clock+	0.0271436 ns	

Table 2. CSI pin delay

Pin #	Pin name	Signal description	Direction	Pin type
213	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3 V on the module.	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	Camera I2C Data. 2.2 kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
116	CAM0_MCLK	Camera 0 Reference Clock	Output	CMOS – 1.8V
114	CAM0_PWDN	Camera 0 Powerdown or GPIO	Output	CMOS – 1.8V
122	CAM1_MCLK	Camera 1 Reference Clock	Output	CMOS – 1.8V
120	CAM1_PWDN	Camera 1 Powerdown or GPIO	Output	CMOS – 1.8V

Table 3. Camera control pin descriptions

- DVP interface
  - One 8/10/12/16-bit standard DVP interface, up to 150 MHz input data
  - Support BT.601/BT.656 and BT.1120 VI interface
  - Support the polarity of pixel_clk, hsync, vsync configurable
- HDMI RX interface
  - Single-port HDMI 2.0 RX PHY, 4 lanes, no sideband channels
  - Data rate support in HDMI 2.0 mode
    - 6 Gbps down to 3.4 Gbps
  - Data rate support in HDMI 1.4 mode
    - 3.4 Gbps down to 250 Mbps
  - HDMI 2.0 video formats
    - TMDS Scrambler to enable support for 2160p@60 Hz with RGB/YCbCr4:4:4 or YCbCr4:2:2
    - Supports YCbCr 4:2:0 to enable 2160p@60 Hz at lower HDMI link speeds
  - HDMI 1.4b video formats
    - All CEA-861-E video formats up to 1080p@120 Hz
    - HDMI 1.4b 4K x 2K video formats (3840 x 2160p@24 Hz/25 Hz/30 Hz and 4096 x 2160p@24 Hz)
    - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)
  - Support HDCP2.3 and HDCP1.4

4.9 Image signal processor

- Video capture (VICAP)

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  - Support BT601, BT656, BT1120
  - Support receiving six interfaces of MIPI CSI/DSI, up to four IDs for each interface
  - Support five CSI data formats: RAW8/10/12/14, YUV422
  - Support three modes of HDR: virtual channel mode, identification code mode, line counter mode
  - Support RAW data through to ISP0/1
- Maximum input
  - 48M: 8064 x 6048@15 dual ISP
  - 32M: 6528 x 4898@30 dual ISP
  - 16M: 4672 x 3504@30 single ISP
- 3A: include AE/Histogram, AF, AWB statistics output
- FPN: Fixed Pattern Noise removal
- BLC: Black Level Correction
- DPCC: Static/Dynamic defect pixel cluster correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens shading correction
- Bayer-2DNR: Spatial Bayer-raw De-noising
- Bayer-3DNR: Temporal Bayer-raw De-noising
- CAC: Chromatic Aberration Correction
- HDR: 3-Frame Merge into High-Dynamic Range
- DRC: HDR Dynamic Range Compression, Tone mapping
- GIC: Green Imbalance Correction
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction
- CCM/CSM: Color correction matrix; RGB2YUV etc
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and Effect enhancement
- 3DLUT: 3D-Lut Color Palette for Customer
- LDCH: Lens-distortion only in the horizontal direction
- YUV-2DNR: Spatial YUV De-noising
- Sharp: Image Sharpening and boundary filtering
- CMSK: privacy mask
- GAIN: image local gain
- Support multi-sensor reuse ISP
- FishEye Correction (FEC)
  - Input mode and data format
    - Support RASTER: YUV422SP, YUV422I, YUV420SP
  - Output mode and data format
    - RASTER: YUV422SP, YUV422I, YUV420SP
    - FBCE: YUV422SP, YUV420SP
  - Support 16 x 8, 32 x 16 two densities
  - Support up to 4 times reduction factor
  - Resolution 128 x 128~4095 x 4095
  - Y Interpolation: Bicubic; C Interpolation: Biliner

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4.10 Display interface

- HDMI TX interface
  - Support one HDMI TX
  - Support 1/2/4 lanes for each interface
  - Support all the data rates: 3, 6, 8, 10 and 12 Gbps
  - Support up to 7680 x 4320@60 Hz
  - Support RGB/YUV (up to 10 bits) format
  - Support DSC 1.2a
  - Support HDCP2.3
- DP/eDP TX interface
  - Support one DP/eDP combo interface
  - Support 1/2/4 lanes for each interface
  - Support 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps for DP
  - Support 1.62 Gbps, 2.7 Gbps, 5.4 Gbps for eDP
  - Support up to 7680 x 4320@60 Hz for DP, 8192 x 4320@30 Hz for eDP
  - Support RGB/YUV (up to 10 bits) format for DP
  - Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format for eDP
  - Support Single Stream Transport (SST) for DP
  - Support HDCP 2.3/HDCP 1.3 for DP, HDCP1.3 for eDP
- MIPI DSI interface
  - Support 2 MIPI DPHY 2.0 interfaces
  - Support 4 data lanes and 4.5 Gbps maximum data rate per lane
  - Support max resolution 4K@60 Hz
  - Support dual MIPI display: left-right mode
  - Support RGB (up to 10 bits) format
  - Support DSC 1.1/1.2a
- BT.1120 video output interface
  - Support up to 1920 x 1080@60 Hz
  - Support RGB (up to 8 bits) format
  - Up to 150 MHz data rate
- Notice
  - In version 2.1.0, the PCB design reversed the positions of the D0 signal and the D2 signal in Display Port 1.

Pin #	Pin name	Signal description	Direction	Pin type
39	DP0_TXD0_N	Display Port 0 Lane 0– & USB3.0 #0 SS Receive–	Input	DP/eDP/USB3.0
41	DP0_TXD0_P	Display Port 0 Lane 0+ & USB3.0 #0 SS Receive+	Input	DP/eDP/USB3.0
45	DP0_TXD1_N	Display Port 0 Lane 1– & USB3.0 #0 SS Transmit–	Output	DP/eDP/USB3.0
47	DP0_TXD1_P	Display Port 0 Lane 1+ & USB3.0 #0 SS Transmit+	Output	DP/eDP/USB3.0
51	DP0_TXD2_N	Display Port 0 Lane 2– & USB3.0 #0 SS Receive–	Input	DP/eDP/USB3.0
53	DP0_TXD2_P	Display Port 0 Lane 2+ & USB3.0 #0 SS Receive+	Input	DP/eDP/USB3.0
57	DP0_TXD3_N	Display Port 0 Lane 3– & USB3.0 #0 SS Transmit–	Output	DP/eDP/USB3.0

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Pin #	Pin name	Signal description	Direction	Pin type
59	DP0_TXD3_P	Display Port 0 Lane 3+ & USB3.0 #0 SS Transmit+	Output	DP/eDP/USB3.0
223	DP0_AUX_P	Display Port 0 Aux+ & USB3.0 #0 SS Sideband+	Bidir	DP/eDP/USB3.0
225	DP0_AUX_N	Display Port 0 Aux– & USB3.0 #0 SS Sideband-	Bidir	DP/eDP/USB3.0
63	DP1_TXD0_N	Display Port 1 Lane 2– & HDMI1 Lane 2–	Output	DP/eDP/HDMI
65	DP1_TXD0_P	Display Port 1 Lane 2+ & HDMI1 Lane 2+	Output	DP/eDP/HDMI
69	DP1_TXD1_N	Display Port 1 Lane 1– & HDMI1 Lane 1–	Output	DP/eDP/HDMI
71	DP1_TXD1_P	Display Port 1 Lane 1+ & HDMI1 Lane 1+	Output	DP/eDP/HDMI
75	DP1_TXD2_N	Display Port 1 Lane 0– & HDMI1 Lane 0–	Output	DP/eDP/HDMI
77	DP1_TXD2_P	Display Port 1 Lane 0+ & HDMI1 Lane 0+	Output	DP/eDP/HDMI
81	DP1_TXD3_N	Display Port 1 Lane 3– & HDMI1 Clk Lane–	Output	DP/eDP/HDMI
83	DP1_TXD3_P	Display Port 1 Lane 3+ & HDMI1 Clk Lane+	Output	DP/eDP/HDMI
98	DP1_AUX_N	Display Port 1 Aux– & HDMI1 DDC SDA	Bidir	Open-Drain, 3.3V
100	DP1_AUX_P	Display Port 1 Aux+ & HDMI1 DDC SCL	Bidir	Open-Drain, 3.3V
96	DP1_HPD	Display Port 1 & HDMI1 Hot Plug Detect	Input	Open Drain – 1.8V
94	HDMI_ CEC	HDMI CEC	Bidir	Open Drain – 3.3V

Table 4. DP/eDP/HDMI pin descriptions

4.11 Video output processor

- Video ports
  - Video Port0, max output resolution: 7680 x 4320@60 Hz
  - Video Port1, max output resolution: 4096 x 2304@60 Hz
  - Video Port2, max output resolution: 4096 x 2304@60 Hz
  - Video Port3, max output resolution: 1920 x 1080@60 Hz
- Cluster 0/1/2/3
  - Max input and output resolution 4096 x 2304
  - Support AFBCD
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 4~1/4
  - Support rotation
- ESMART 0/1/2/3
  - Max input and output resolution 4096 x 2304
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 8~1/8
  - Support 4 regions
  - Overlay
    - Support up to 8 layers overlay: 4 cluster/4 esmart
    - Support RGB/YUV domain overlay
- Post process
  - HDR

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        - HDR10/HDR HLG
        - HDR2SDR/SDR2HDR
    - 3D-LUT/P2I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR
- Write back
    - Format: ARGB8888/RGB888/RGB565/YUV420
    - Max resolution: 1920 x 1080

4.12 Audio interface

- I^2S0/I^2S1 with 8 channels
    - Up to 8 channels TX and 8 channels RX path
    - Audio resolution from 16 bits to 32 bits
    - Sample rate up to 192 KHz
    - Provides master and slave work mode, software configurable
    - Support 3 I^2S formats (normal, left-justified, right-justified)
    - Support 4 PCM formats (early, late1, late2, late3)
    - Support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
    - I^2S, PCM and TDM mode cannot be used at the same time
- I^2S2/I^2S3 with 2 channels
    - Up to 2 channels for TX and 2 channels for RX path
    - Audio resolution from 16 bits to 32 bits
    - Sample rate up to 192 KHz
    - Provides master and slave work mode, software configurable
    - Support 3 I^2S formats (normal, left-justified, right-justified)
    - Support 4 PCM formats (early, late1, late2, late3)
    - I^2S and PCM cannot be used at the same time
- SPDIF0/SPDIF1
    - Support two 16-bit audio data store together in one 32-bit wide location
    - Support bi-phase format stereo audio data output
    - Support 16- to 31-bit audio data left or right justified in 32-bit wide sample data buffer
    - Support 16-, 20-, 24-bit audio data transfer in linear PCM mode
    - Support non-linear PCM transfer
- PDM0/PDM1
    - Up to 8 channels
    - Audio resolution from 16 bits to 24 bits
    - Sample rate up to 192 KHz
    - Support PDM master receive mode
- Digital Audio Codec
    - Support 2 channels digital DAC
    - Support I^2S/PCM interface, master and slave mode
    - Support 16-bit sample resolution
    - Support three modes of mixing for every digital DAC channel
    - Support volume control

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- VAD (Voice Activity Detection)
  - Support read voice data from I²S/PDM
  - Support voice amplitude detection
  - Support Multi-Mic array data storing
  - Support a level combined interrupt

Pin #	Pin name	Signal description	Direction	Pin type
193	I2S0_DOUT	I2S Audio Port 0 Data Out	Output	CMOS – 1.8V
195	I2S0_DIN	I2S Audio Port 0 Data In	Input	CMOS – 1.8V
197	I2S0_FS	I2S Audio Port 0 Left/Right Clock	Bidir	CMOS – 1.8V
199	I2S0_SCLK	I2S Audio Port 0 Clock	Bidir	CMOS – 1.8V
220	I2S1_DOUT	I2S Audio Port 1 Data Out	Output	CMOS – 1.8V
222	I2S1_DIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V
224	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V
226	I2S1_SCLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
124	I2S2_DOUT	I2S Audio Port 2 Data Out	Output	CMOS – 1.8V
126	I2S2_DIN	I2S Audio Port 2 Data In	Input	CMOS – 1.8V
127	I2S2_FS	I2S Audio Port 2 Left/Right Clock	Bidir	CMOS – 1.8V
128	I2S2_SCLK	I2S Audio Port 2 Clock	Bidir	CMOS – 1.8V
112	I2S3_DIN	I2S Audio Port 3 Data In	Input	CMOS – 1.8V
130	I2S3_FS	I2S Audio Port 3 Left/Right Clock	Bidir	CMOS – 1.8V
218	I2S3_DOUT	I2S Audio Port 3 Data Out	Output	CMOS – 1.8V
212	I2S3_SCLK	I2S Audio Port 3 Clock	Bidir	CMOS – 1.8V

Table 5. I²S audio pin descriptions

4.13 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus width

- GMAC 10/100/1000M Ethernet controller
  - Support two Ethernet controllers
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex operation

Pin #	Pin name	Signal description	Direction	Pin type
184	GBE_MDI0_N	GbE Transformer Data 0–	Bidir	MDI

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186	GBE_MDI0_P	GbE Transformer Data 0+	Bidir	MDI
190	GBE_MDI1_N	GbE Transformer Data 1–	Bidir	MDI
192	GBE_MDI1_P	GbE Transformer Data 1+	Bidir	MDI
196	GBE_MDI2_N	GbE Transformer Data 2–	Bidir	MDI
198	GBE_MDI2_P	GbE Transformer Data 2+	Bidir	MDI
202	GBE_MDI3_N	GbE Transformer Data 3–	Bidir	MDI
204	GBE_MDI3_P	GbE Transformer Data 3+	Bidir	MDI
188	GBE_LED_LINK	Ethernet Link LED (Green)	Output	-
194	GBE_LED_ACT	Ethernet Activity LED (Yellow)	Output	-

Table 6. Gigabit Ethernet pin descriptions

- USB 3.0
  - Embedded two USB 3.0 OTG interfaces which combo with DP TX (USB3OTG_0 and USB3OTG_1)
  - Embedded one USB 3.0 Host interface which combos with Combo PIPE PHY2 (USB3OTG_2)
  - Compatible Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG_2)
    - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Simultaneous IN and OUT transfer for USB 3.0, up to 8 Gbps bandwidth
  - Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  - LPM protocol in USB 2.0 (exclude USB3OTG_2) and U0, U1, U2, and U3 states for USB 3.0
  - USB 3.0 device features
    - Up to 10 IN endpoints, including control endpoint 0
    - Up to 6 OUT endpoints, including control endpoint 0
    - Up to 16 endpoint transfer resources, each one for each endpoint
    - Flexible endpoint configuration for multiple applications/USB set-configuration modes
    - Hardware handles ERDY and burst
    - Stream-based bulk endpoints with controller automatically initiating data movement
    - Isochronous endpoints with isochronous data in data buffers
    - Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
  - USB 3.0 xHCI host features
    - Support up to 64 devices
    - Support one interrupter
    - Support one USB 2.0 port (exclude USB3OTG_2) and one Super-Speed port
    - Support standard or open-source xHCI and class driver
  - USB 3.0 Dual-Role Device (DRD) Features
    - Static Device Operation
    - Static Host Operation

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- ◆ USB 3.0/USB 2.0 OTG A device and B device basing on ID, USB3OTG_2 only support USB 3.0
- ◆ Not Support USB 3.0/USB 2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)

- Miscellaneous features
  - ◆ USB 2.0 PHY support Battery Charge detection
  - ◆ USB3OTG_0 and USB3OTG_1 support USB Type-C and DP Alt Mode
  - ◆ USB3OTG_2 PHY combos with PCIe and SATA

Pin #	Pin name	Signal description	Direction	Pin type
161	USBSS_RX_N	USB3.0 #1 SS Receive–	Input	USB3.0
163	USBSS_RX_P	USB3.0 #1 SS Receive+	Input	USB3.0
166	USBSS_TX_N	USB3.0 #1 SS Transmit–	Output	USB3.0
168	USBSS_TX_P	USB3.0 #1 SS Transmit+	Output	USB3.0

Table 7. USB 3.0 pin descriptions

- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Support two USB 2.0 Hosts
  - Supports high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

Pin #	Pin name	Signal description	Direction	Pin type
109	USB0_D_N	USB2.0 Port 0 Data–	Bidir	USB2.0 PHY
111	USB0_D_P	USB2.0 Port 0 Data+	Bidir	USB2.0 PHY
115	USB1_D_N	USB2.0 Port 1 Data–	Bidir	USB2.0 PHY
117	USB1_D_P	USB2.0 Port 1 Data+	Bidir	USB2.0 PHY
121	USB2_D_N	USB2.0 Port 2 Data–	Bidir	USB2.0 PHY
123	USB2_D_P	USB2.0 Port 2 Data+	Bidir	USB2.0 PHY

Table 8. USB 2.0 pin descriptions

- Combo PIPE PHY Interface
  - Support three Combo PIPE PHYs with PCIe 2.1/SATA 3.0/USB 3.0 controller
- Combo PIPE PHY0 supports one of the following interfaces:
  - SATA
  - PCIe 2.1
- Combo PIPE PHY1 supports one of the following interfaces:
  - SATA
  - PCIe 2.1
- Combo PIPE PHY2 supports one of the following interfaces:
  - SATA

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- PCIe 2.1
- USB 3.0

- PCIe 2.1 interface
  - Compatible with PCI Express Base Specification Revision 2.1
  - Support one lane for each PCIe 2.1 interface
  - Support Root Complex (RC) only
  - Support 5 Gbps data rate

Pin #	Pin name	Signal description	Direction	Pin type
167	PCIE1_RX0_N	PCIe2.0 #1 Receive 0–	Input	PCIe PHY
169	PCIE1_RX0_P	PCIe2.0 #1 Receive 0+	Input	PCIe PHY
172	PCIE1_TX0_N	PCIe2.0 #1 Transmit 0–	Output	PCIe PHY
174	PCIE1_TX0_P	PCIe2.0 #1 Transmit 0+	Output	PCIe PHY
183	PCIE1_RST*	PCIe2.0 #1 Reset. 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain – 3.3V
182	PCIE1_CLKREQ*	PCIe2.0 #1 Clock Request. 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
173	PCIE1_CLK_N	PCIe2.0 #1 Reference Clock–	Output	PCIe PHY
175	PCIE1_CLK_P	PCIe2.0 #1 Reference Clock+	Output	PCIe PHY
179	PCIE_WAKE*	PCIe Wake. 47kΩ pull-up to 3.3V on the module.	Input	Open Drain – 3.3V
40	PCIE2_RX0_N	PCIe2.0 #2 Receive 0–	Input	PCIe PHY
42	PCIE2_RX0_P	PCIe2.0 #2 Receive 0+	Input	PCIe PHY
46	PCIE2_TX0_N	PCIe2.0 #2 Transmit 0–	Output	PCIe PHY
48	PCIE2_TX0_P	PCIe2.0 #2 Transmit 0+	Output	PCIe PHY
52	PCIE2_CLK_N	PCIe2.0 #2 Reference Clock–	Output	PCIe PHY
54	PCIE2_CLK_P	PCIe2.0 #2 Reference Clock+	Output	PCIe PHY
219	PCIE2_RST*	PCIe2.0 #2 Reset. 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain – 3.3V
221	PCIE2_CLKREQ*	PCIe2.0 #2 Clock Request. 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V

Table 9. PCIe 2.1 pin descriptions

- SATA interface
  - Compatible with Serial ATA 3.1 and AHCI revision 1.3.1
  - Support eSATA
  - Support one port for each SATA interface
  - Support 6 Gbps data rate
- PCIe 3.0 interface
  - Compatible with PCI Express Base Specification Revision 3.0
  - Support dual operation modes: Root Complex (RC) and End Point (EP)

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- Support data rates: 2.5 Gbps (PCIe 1.1), 5 Gbps (PCIe 2.1), 8 Gbps (PCIe 3.0)
- Support aggregation and bifurcation with 1x 4 lanes, 2x 2 lanes, 4x 1 lanes and 1x 2 lanes + 2x 1 lanes

Pin #	Pin name	Signal description	Direction	Pin type
131	PCIE0_RX0_N	PCIe3.0 #0 Receive 0– (PCIe Ctrl #0 Lane 0)	Input	PCIe PHY
133	PCIE0_RX0_P	PCIe3.0 #0 Receive 0+ (PCIe Ctrl #0 Lane 0)	Input	PCIe PHY
134	PCIE0_TX0_N	PCIe3.0 #0 Transmit 0– (PCIe Ctrl #0 Lane 0)	Output	PCIe PHY
136	PCIE0_TX0_P	PCIe3.0 #0 Transmit 0+ (PCIe Ctrl #0 Lane 0)	Output	PCIe PHY
137	PCIE0_RX1_N	PCIe3.0 #0 Receive 1– (PCIe Ctrl #0 Lane 1)	Input	PCIe PHY
139	PCIE0_RX1_P	PCIe3.0 #0 Receive 1+ (PCIe Ctrl #0 Lane 1)	Input	PCIe PHY
140	PCIE0_TX1_N	PCIe3.0 #0 Transmit 1– PCIe Ctrl #0 Lane 1)	Output	PCIe PHY
142	PCIE0_TX1_P	PCIe3.0 #0 Transmit 1+ (PCIe Ctrl #0 Lane 1)	Output	PCIe PHY
149	PCIE0_RX2_N	PCIe3.0 #1 Receive 2– (PCIe Ctrl #1 Lane 2)	Input	PCIe PHY
151	PCIE0_RX2_P	PCIe3.0 #1 Receive 2+ (PCIe Ctrl #1 Lane 2)	Input	PCIe PHY
148	PCIE0_TX2_N	PCIe3.0 #1 Transmit 2– (PCIe Ctrl #1 Lane 2)	Output	PCIe PHY
150	PCIE0_TX2_P	PCIe3.0 #1 Transmit 2+ (PCIe Ctrl #1 Lane 2)	Output	PCIe PHY
155	PCIE0_RX3_N	PCIe3.0 #1 Receive 3– (PCIe Ctrl #1 Lane 3)	Input	PCIe PHY
157	PCIE0_RX3_P	PCIe3.0 #1 Receive 3+ (PCIe Ctrl #1 Lane 3)	Input	PCIe PHY
154	PCIE0_TX3_N	PCIe3.0 #1 Transmit 3– PCIe Ctrl #1 Lane 3)	Output	PCIe PHY
156	PCIE0_TX3_P	PCIe3.0 #1 Transmit 3+ (PCIe Ctrl #1 Lane 3)	Output	PCIe PHY
181	PCIE0_RST*	PCIe3.0 #0 Reset. 4.7kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
180	PCIE0_CLKREQ*	PCIe3.0 Clock Request. 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
179	PCIE_WAKE*	PCIe Wake. 47kΩ pull-up to 3.3V on the module.	Input	Open Drain – 3.3V
160	PCIE0_CLK_N	PCIe3.0 Reference Clock–	Output	PCIe PHY
162	PCIE0_CLK_P	PCIe3.0 Reference Clock+	Output	PCIe PHY
229	PCIE30_PORT0_CLKN	PCIe3.0 Port 0 Reference Clock–	Output	PCIe PHY
227	PCIE30_PORT0_CLKP	PCIe3.0 Port 0 Reference Clock+	Output	PCIe PHY

Table 10. PCIe 3.0 pin descriptions

- SPI interface
  - Support 5 SPI Controllers (SPI0-SPI4)
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

Pin #	Pin name	Signal description	Direction	Pin type
91	SPI0_SCK	SPI 1 Clock	Bidir	CMOS – 1.8V

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Pin #	Pin name	Signal description	Direction	Pin type
89	SPI0_MOSI	SPI 1 Master Out / Slave In	Bidir	CMOS – 1.8V
93	SPI0_MISO	SPI 1 Master In / Slave Out	Bidir	CMOS – 1.8V
95	SPI0_CS0*	SPI 1 Chip Select 0	Bidir	CMOS – 1.8V
97	SPI0_CS1*	SPI 1 Chip Select 1	Bidir	CMOS – 1.8V
104	SPI1_MOSI	SPI 0 Master Out / Slave In	Bidir	CMOS – 1.8V
106	SPI1_SCK	SPI 0 Clock	Bidir	CMOS – 1.8V
108	SPI1_MISO	SPI 0 Master In / Slave Out	Bidir	CMOS – 1.8V
110	SPI1_CS0*	SPI 0 Chip Select 0	Bidir	CMOS – 1.8V

Table 11. SPI pin descriptions

- I^2C Master controller
  - Support 9 I^2C master (I^2C0-I^2C8)
  - Support 7-bit and 10-bit address mode
  - Software programmable clock frequency
  - Data on the I^2C-bus can be transferred at rates of up to 100 Kbps in the Standard-mode, up to 400 Kbps in the Fast-mode

Pin #	Pin name	Signal description	Direction	Pin type
185	I2C0_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	Bidir	Open Drain –3.3V
187	I2C0_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain –3.3V
189	I2C1_SCL	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain –3.3V
191	I2C1_SDA	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain –3.3V
232	I2C2_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain –1.8V
234	I2C2_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain –1.8V
213	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain –3.3V
215	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain –3.3V

Table 12. I^2C pin descriptions

- UART interface
  - Support 10 UART interfaces (UART0-UART9)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support transmitting or receiving 5-bit, 6-bit, 7-bit, and 8-bit serial data
  - Standard asynchronous communication bits such as start, stop and parity

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- Support different input clocks for UART operation to get up to 4 Mbps baud rate
- Support auto flow control mode for all UART interfaces

Pin #	Pin name	Signal description	Direction	Pin type
99	UART0_TXD	UART #0 Transmit	Output	CMOS – 1.8V
101	UART0_RXD	UART #0 Receive	Input	CMOS – 1.8V
103	UART0_RTS*	UART #0 Request to Send	Output	CMOS – 1.8V
105	UART0_CTS*	UART #0 Clear to Send	Input	CMOS – 1.8V
203	UART1_TXD	UART #1 Transmit	Output	CMOS – 1.8V
205	UART1_RXD	UART #1 Receive	Input	CMOS – 1.8V
207	UART1_RTS*	UART #1 Request to Send	Output	CMOS – 1.8V
209	UART1_CTS*	UART #1 Clear to Send	Input	CMOS – 1.8V
236	UART2_TXD	UART #2 Transmit	Output	CMOS – 1.8V
238	UART2_RXD	UART #2 Receive	Input	CMOS – 1.8V

Table 13. UART pin descriptions

- CAN bus
  - Support 3 CAN buses
  - Support CAN 2.0B protocol
  - Support transmitting or receiving CAN standard frame
  - Support transmitting or receiving CAN extended frame
  - Support transmitting or receiving data frame, remote frame, overload frame, error frame, and frame interval

Pin #	Pin name	Signal description	Direction	Pin type
145	CAN_TX	CAN PHY	Output	CMOS – 3.3V
143	CAN_RX	CAN PHY	Input	CMOS – 3.3V

Table 14. CAN pin descriptions

4.14 Others

- Multiple groups of GPIOs
  - All GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable drive strength

Pin #	Pin name	Signal description	Direction	Pin type

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Pin #	Pin name	Signal description	Direction	Pin type
87	GPIO00	GPIO #0 or USB 0 VBUS Enable #0	Bidir	CMOS – 1.8V
118	GPIO01	GPIO #1 or Generic Clocks	Bidir	CMOS – 1.8V
206	GPIO07	GPIO #7 or Pulse Width Modulator	Bidir	CMOS – 1.8V
208	GPIO08	GPIO #8 or Fan Tach	Bidir	CMOS – 1.8V
211	GPIO09	GPIO #9 or Audio Codec Master Clock	Bidir	CMOS – 1.8V
216	GPIO11	GPIO #11 or Generic Clocks	Bidir	CMOS – 1.8V
228	GPIO13	GPIO #13 or Pulse Width Modulator	Bidir	CMOS – 1.8V
230	GPIO14	GPIO #14 or Pulse Width Modulator	Bidir	CMOS – 1.8V
92	GPIO15	GPIO #15 or USB 1 VBUS Enable #1	Bidir	CMOS – 3.3V

Table 15. GPIO pin descriptions

- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support up to 7 channels TS-ADC, the temperature criteria of each channel can be configurable
  - -40~125°C temperature range and 1°C temperature resolution
- Successive approximation register ADC (SAR ADC)
  - 12-bit resolution
  - Up to 1 MS/s sampling rate
  - Eight single-ended input channels
- OTP
  - Support 32 Kbit address space and the higher 4 Kbit address space is non-secure part
  - Support read and program word mask in secure model
  - Support maximum 32-bit OTP program operation
  - Support maximum 16-word OTP read operation
  - Program and Read state can be read
  - Program fail address record
- Package type
  - FCBGA1088L (body: 23 mm x 23 mm; ball size: 0.36 mm; ball pitch: 0.65 mm)

5. Power and system management

5.1 Power and system management

VIN must be supplied by the carrier board that the module is designed to connect to. All interfaces are referenced to on-module voltage rails, additional I/O voltage is not required to be supplied to

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the module.

Pin #	Pin name	Signal description	Direction	Pin type
251 252 253 254 255 256 257 258 259 260	VDD_IN	Main power – Supplies PMIC and other registers	Input	5.0V
235	PMIC_BBAT	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Bidir	1.65V-5.5V
233	SHUTDOWN_REQ*	Used by the module to request a shutdown from the carrier board. Pull up to VDD_IN_5V with 4.7 kΩ on the module.	Output	Analog –5.0V
237	POWER_EN	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on themodule. A 45 kΩ pullup is in the PMIC.	Input	CMOS –5.0V
239	SYS_RESET*	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. Pull up to 1.8 V with 10 kΩ resistor on the module.	Bidir	Open Drain – 1.8V
178	MOD_SLEEP*	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	Output	CMOS –3.3V
210	CLK_32K_OUT	Sleep/Suspend clock	Output	CMOS –1.8V
214	FORCE_RECOVERY*	Force Recovery strap pin	Input	CMOS –1.8V
240	SLEEP/WAKE*	Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	Input	CMOS –5.0V

Table 16. Power and system control pin descriptions

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5.2 PMC

The power management controller (PMC) power management features enable both high speed operation and very low-power standby states. The PMC primarily controls voltage transitions for the SoC as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I^2C, RTC, USB) which can wake the system from deep sleep state. The PMC enables aggressive power-gating capabilities on idle modules and integrates specific logic to maintain defined states and control power domains during sleep and deep sleep modes.

5.3 Resets

If you assert reset, the Mixtile Core 3588E and onboard storage will be reset. This signal is also used for baseboard power sequencing.

5.4 PMIC_BBAT

An optional backup battery can be attached to the VCC_RTC module input to maintain the module RTC when VIN is not present. This pin is connected directly to the onboard PMIC. Details of the types of backup cells that optionally can be connected are found in the PMIC manufacturer's data sheet. When a backup cell is connected to the PMIC, the RTC retains its contents and can be configured to charge the backup cell as well. RTC accuracy is 2 seconds/day in typical room temperature only.
The following backup cells may be attached to this pin:

- Super capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells
  The backup cells must provide a voltage in the range 2.5 V to 3.5 V.

5.5 Power sequencing

Mixtile Core 3588E is required to be powered on and off in a known sequence. Sequencing is determined through a set of control signals; the SYS_RESET* signal (when deasserted) is used to indicate when the carrier board can power on. The following sections provide an overview of the power sequencing steps between the carrier board and Mixtile Core 3588E. The Mixtile Core 3588E and the product carrier board must be power sequenced properly to avoid potential damage to components on either the module or the carrier board system.

5.5.1 Power up

During power-up, the carrier board must wait until the signal SYS_RESET* is deasserted from the Mixtile Core 3588E before enabling its power; the Mixtile Core 3588E deasserts the SYS_RESET* signal to enable the complete system to boot.

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5.5.2 Power down

Shutdown events can be triggered by either the module or the baseboard, but the shutdown event is always serviced by the baseboard. To do so, the baseboard deasserts POWER_EN, which begins the shutdown power sequence on the module. If the module needs to request a shutdown event in the case of thermal, software, or under-voltage events, it asserts SHUTDOWN_REQ*. When the baseboard sees low SHUTDOWN_REQ*, it should deassert POWER_EN as soon as possible.
Once POWER_EN is deasserted, the module asserts SYS_RESET*, and the baseboard may shut down. SoC 3.3 V I/O must reach 0.5 V or lower at most 1.5 ms after SYS_RESET* is asserted. SoC 1.8 V I/O must reach 0.5 V or lower at most 4 ms after SYS_RESET* is asserted.

6. Block diagram

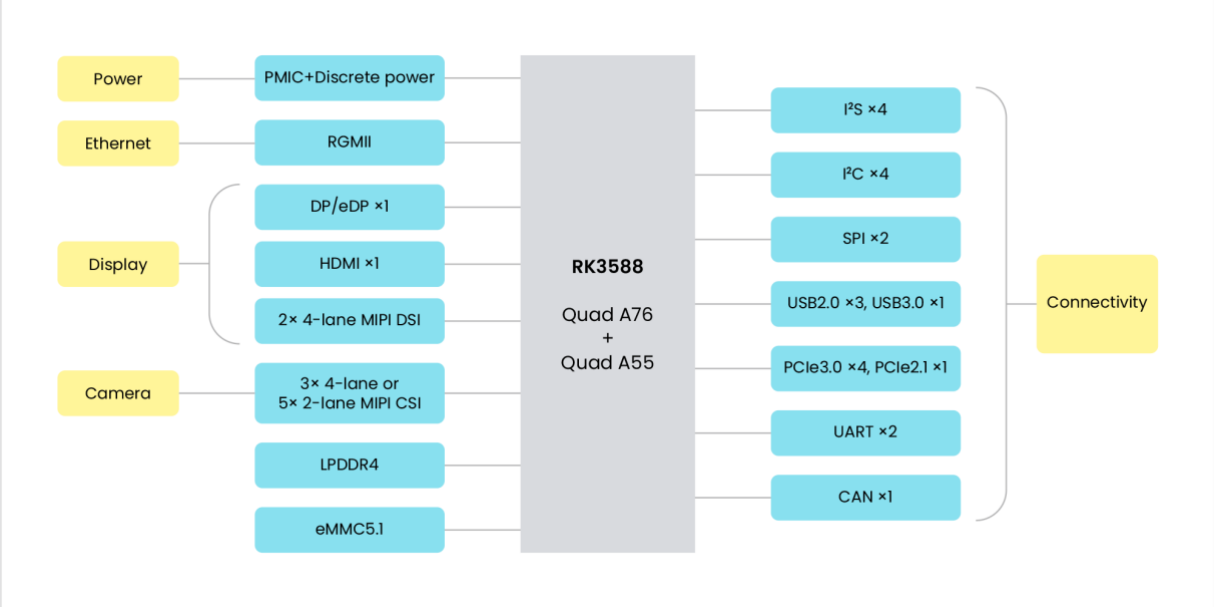


Figure 3. Block diagram of Core 3588E

Figure 4. Physical dimensions of Core 3588E

7. Pin definition

The following table lists the pin definition of Core 3588E.
Notice:

- The signal of the CSI0 port is connected to the definition of the CSI1 interface, while the signal of the CSI1 port is connected to the definition of the CSI0 interface.
- The D0 signal of the DP1 port is connected to the D2 interface, and the D2 signal is connected to the D0 interface.

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Core 3588E function	Pin number	Pin number	Core 3588E function
GND_1	1	2	GND_2
CSI1_D0_N	3	4	CSI0_D0_N
CSI1_D0_P	5	6	CSI0_D0_P
GND_3	7	8	GND_4
CSI1_CLK_N	9	10	CSI0_CLK_N
CSI1_CLK_P	11	12	CSI0_CLK_P
GND_5	13	14	GND_6
CSI1_D1_N	15	16	CSI0_D1_N
CSI1_D1_P	17	18	CSI0_D1_P
GND_7	19	20	GND_8
CSI3_D0_N	21	22	CSI2_D0_N
CSI3_D0_P	23	24	CSI2_D0_P
GND_9	25	26	GND_10
CSI3_CLK_N	27	28	CSI2_CLK_N
CSI3_CLK_P	29	30	CSI2_CLK_P
GND_11	31	32	GND_12
CSI3_D1_N	33	34	CSI2_D1_N
CSI3_D1_P	35	36	CSI2_D1_P
GND_13	37	38	GND_14
DP0_TXD0_N	39	40	PCIE2_RX0_N
DP0_TXD0_P	41	42	PCIE2_RX0_P
GND_15	43	44	GND_16
DP0_TXD1_N	45	46	PCIE2_TX0_N
DP0_TXD1_P	47	48	PCIE2_TX0_P
GND_17	49	50	GND_18
DP0_TXD2_N	51	52	PCIE2_CLK_N
DP0_TXD2_P	53	54	PCIE2_CLK_P
GND_19	55	56	GND_20
DP0_TXD3_N	57	58	CSI4_D0_N
DP0_TXD3_P	59	60	CSI4_D0_P
GND_21	61	62	GND_22
DP1_TXD0_N	63	64	CSI4_D1_N
DP1_TXD0_P	65	66	CSI4_D1_P
GND_23	67	68	GND_24
DP1_TXD1_N	69	70	CSI4_CLK_N
DP1_TXD1_P	71	72	CSI4_CLK_P
GND_25	73	74	GND_26
DP1_TXD2_N	75	76	CSI5_D0_N
DP1_TXD2_P	77	78	CSI5_D0_P
GND_27	79	80	GND_28

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DP1_TXD3_N	81	82	CSI5_D1_N
DP1_TXD3_P	83	84	CSI5_D1_P
GND_29	85	86	GND_30
GPIO00	87	88	CSI5_CLK_N
SPI0_MOSI	89	90	CSI5_CLK_P
SPI0_SCK	91	92	GPIO15
SPI0_MISO	93	94	HDMI_CEC
SPI0_CS0	95	96	DP1_HPD
SPI0_CS1	97	98	DP1_AUX_N
UART0_TXD	99	100	DP1_AUX_P
UART0_RXD	101	102	GND_31
UART0_RTS	103	104	SPI1_MOSI
UART0_CTS	105	106	SPI1_SCK
GND_32	107	108	SPI1_MISO
USB0_D_N	109	110	SPI1_CS0
USB0_D_P	111	112	I2S3_DIN
GND_33	113	114	CAM0_PWDN
USB1_D_N	115	116	CAM0_MCLK
USB1_D_P	117	118	GPIO01
GND_34	119	120	CAM1_PWDN
USB2_D_N	121	122	CAM1_MCLK
USB2_D_P	123	124	I2S2_DOUT
GND_35	125	126	I2S2_DIN
I2S2_FS	127	128	I2S2_SCLK
GND_36	129	130	I2S3_FS
PCIE0_RX0_N	131	132	GND_37
PCIE0_RX0_P	133	134	PCIE0_TX0_N
GND_38	135	136	PCIE0_TX0_P
PCIE0_RX1_N	137	138	GND_39
PCIE0_RX1_P	139	140	PCIE0_TX1_N
GND_40	141	142	PCIE0_TX1_P
CAN_RX	143	144	GND_41
CAN_TX	145	146	GND_42
GND_43	147	148	PCIE0_TX2_N
PCIE0_RX2_N	149	150	PCIE0_TX2_P
PCIE0_RX2_P	151	152	GND_44
GND_45	153	154	PCIE0_TX3_N
PCIE0_RX3_N	155	156	PCIE0_TX3_P
PCIE0_RX3_P	157	158	GND_46
GND_47	159	160	PCIE0_CLK_N
USBSS_RX_N	161	162	PCIE0_CLK_P
USBSS_RX_P	163	164	GND_48

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GND_49	165	166	USBSS_TX_N
PCIE1_RX0_N	167	168	USBSS_TX_P
PCIE1_RX0_P	169	170	GND_50
GND_51	171	172	PCIE1_TX0_N
PCIE1_CLK_N	173	174	PCIE1_TX0_P
PCIE1_CLK_P	175	176	GND_52
GND_53	177	178	MOD_SLEEP
PCIE_WAKE	179	180	PCIE0_CLKREQ
PCIE0_RST	181	182	PCIE1_CLKREQ
PCIE1_RST	183	184	GBE_MDI0_N
I2C0_SCL	185	186	GBE_MDI0_P
I2C0_SDA	187	188	GBE_LED_LINK
I2C1_SCL	189	190	GBE_MDI1_N
I2C1_SDA	191	192	GBE_MDI1_P
I2S0_DOUT	193	194	GBE_LED_ACT
I2S0_DIN	195	196	GBE_MDI2_N
I2S0_FS	197	198	GBE_MDI2_P
I2S0_SCLK	199	200	GND_54
GND_55	201	202	GBE_MDI3_N
UART1_TXD	203	204	GBE_MDI3_P
UART1_RXD	205	206	GPIO07
UART1_RTS	207	208	GPIO08
UART1_CTS	209	210	CLK_32K_OUT
GPIO09	211	212	I2S3_SCLK
CAM_I2C_SCL	213	214	FORCE_RECOVERY
CAM_I2C_SDA	215	216	GPIO11
MODULE_ID	217	218	I2S3_DOUT
PCIE2_RST	219	220	I2S1_DOUT
PCIE2_CLKREQ	221	222	I2S1_DIN
DP0_AUX_P	223	224	I2S1_FS
DP0_AUX_N	225	226	I2S1_SCLK
PCIE30_PORT0_CLKP	227	228	GPIO13
PCIE30_PORT0_CLKN	229	230	GPIO14
GND_57	231	232	I2C2_SCL
SHUTDOWN_REQ	233	234	I2C2_SDA
PMIC_BBAT	235	236	UART2_TXD
POWER_EN	237	238	UART2_RXD
SYS_RESET	239	240	SLEEP/WAKE
GND_58	241	242	GND_59
GND_60	243	244	GND_61
GND_62	245	246	GND_63
GND_64	247	248	GND_65

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GND_66	249	250	GND_67
VDD_IN_1	251	252	VDD_IN_2
VDD_IN_3	253	254	VDD_IN_4
VDD_IN_5	255	256	VDD_IN_6
VDD_IN_7	257	258	VDD_IN_8
VDD_IN_9	259	260	VDD_IN_10

8. Technical support

MIXTILE technical support team assists you with the questions you may have. Contact us with the following methods below.

- Email: support@mixtile.com
- Website: https://www.mixtile.com
- Community: https://community.mixtile.com/

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